

**Amendments to the Specification:**

1. Please replace paragraph [0015] with the following amended paragraph:

“According to the claimed invention, ~~apartially a partially~~ depleted SOI MOS device is disclosed. The partially depleted SOI MOS device comprises a silicon wafer having a thin film body, a supporting substrate, and a buried oxide layer isolating the thin film body from the supporting substrate. The thin film body has a main surface. Oxide filled trenches, which extend downwards from the main surface as far as the buried layer, are provided. The trenches are disposed so as to fully enclose a volume of the thin film body, thereby forming a well on the main surface. A dielectric layer is disposed on the main surface. A polysilicon gate of first conductivity type is patterned on the dielectric layer. The polysilicon gate having two opposing long sides that extend from a first end over a first oxide filled trench across the well to a second end, wherein a portion of one of the ends of the polysilicon gate is implanted with ions of second conductivity type opposite to the first conductivity type, whereby a tunneling connection is formed between the well and the implanted portion of the polysilicon gate. Source and drain regions of first conductivity type is formed on opposite sides of the polysilicon gate.”

2. Please replace paragraph [0030] with the following amended paragraph:

“A conventional lithographic process and an ion implantation process are carried out to form an N-well 13 in the P-type silicon thin film 16. More specifically, the PD SOI PMOS device according to the second preferred embodiment of the present invention is fabricated within the N-well 13. After well implantation, active areas (AA) are defined. The PD SOI MOS device according to the second preferred embodiment of the present invention comprises oxide filled STI trenches that extend downwards from the main surface of the silicon thin film 16 as far as the buried oxide layer (not shown) in the SOI substrate. The STI trenches are disposed so as to fully enclose a volume of the thin film body 16, thereby forming a well on the main surface of the thin film body 16. A gate dielectric layer is disposed on the well. A polysilicon gate

33 is disposed on the dielectric layer. The polysilicon gate 33 having two opposing long sides that extend from a first end 36 over a first oxide filled trench across the well to a second end 37 over a [[first]] second oxide filled trench. A portion of each of the ends 36 and 37 of the polysilicon gate 33 is implanted with N type ions. The  
5 implantation may be carried out using a photo mask having a window 60 exposing the portions of the polysilicon gate 33 that directly overlie the extended N type body region 52. The rest portion of the polysilicon gate 33 is implanted with P type ions using a suitable mask. A tunneling connection is formed between the well and the implanted portion of the polysilicon gate 33. P<sup>+</sup> source and drain regions are formed  
10 on opposite sides of the polysilicon gate 33.”